Introduction

Tri-Gate Transistors:
Tri-gate transistors (i.e., fully depleted silicon-on-insulator & integrated transistor consisting of three gates) are basically novel advanced MOS devices which are developed for prolonging the functionality of CMOS technology (transparency & flexibility) and for current down-scaling trend.

Today’s technology is altering very swiftly to maintain stride with Moore’s law for which the dimension of cell is further minimized and additional scaling of transistor is being done for better packaging on a given chip.

In order to improve the short channel resistance and stability, a tri-gate transistor is required. The configuration of tri-gate transistor is designed in a way that they are fully depleted due to which even before reaching the threshold point, the complete silicon present under the gate electrode is depleted of carriers.

Tri-gate transistors have shown expressively developed electronics in terms of sub-threshold slope, gate induced barrier lowering & better scalability as compared to planar single gate transistors.

The tri-gate transistor structure employs low aspect ratio channel channel to deliver conventional conduit for CMOS scaling to the end of roadmap [1] [2]. This structure provides the benefits of tri-gate transistor with the advantages of planar MOSFET. The magnitudes of tri-gate transistor design are very flexible in comparison with single gate transistors and double gate transistors. It also plays a vital role in defining the V-I characteristics [3] & [4].

Structure and Types

There are hundreds of chips inside every wafer of Silicon. Every transistor comprises of two sections: drain and source. In fact, every chip consists of millions of transistors.

There are conducting conduits on the three vases of the vertical pin in a tri-gate transistor. It consists of a single gate electrode on the top and two gate electrodes on the vases. Due to this structure, the control of the gate improves in such a way that even in the “ON” state current flows through it as much as possible.

Also in the “OFF” state, the current flow is practically zero. This phenomenon increases the switching rate between the two states, which outcomes in an enhanced performance for the transistor [7].

Adding to it, the performance benefit can be provided by the control of the nominal width of the conducting conduit [8]. This width is higher in tri-gate transistor because it increases in the 3D structure. This is the major variance between 2D Planar and 3D tri-gate transistors.

But the overall footprint of the transistor remains constant which is illustrated in Figure 1.

Structure and Types

Figure 1: Tri-Gate Transistors [6]

(a) Dual-gate SOI MOSFET. Here we can clearly observe the hard mask. It is a dense dielectric that inhibits the creation of an inversion channel over the top of the silicon (fin). The controllability of the gate is applied on the conduction from the edges of the device.

(b) Tri-gate SOI MOSFET. The control of the gate is applied on the conduction from all three edges of the device (left, right and top).

(c) Gate SOI MOSFET. The control of the gate is advanced over tri-gate MOSFET which is shown in (b) because the electric field across the edges of the gate applies some control on the bottommost edge of the channel (d).

(d) Gate SOI MOSFET. The control of the gate on the bottommost edge of the channel is much better than –gate SOFET. The shape of the gate is represented by names like (gate and name).

(e) SOI MOSFET (gate all around). The control of the gate is applied on the conduit from all four edges of the device. In this scenario, under the channel of silicon, no submerged oxide exists.

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Structure and Types

Figure 2: Effective Channel width for both transistors (6)

Figure 3: Different Forms of Tri-Gate Transistors [6]

(a) Usually tri-gate transistors can also be fabricated on Silicon (SOI) which is also called as a standard bulk substrate. Figure 2 explains several means by which the gate electrode can be enveloped across the channel area of a transistor.

(b) Fabrication Practice of Tri-Gate Transistor (6)

As we can see in the Figure 3 from step (a) to step (d), firstly a layer of insulator is applied at the start of process. We begin with SOI which is the most considered step used for tri-gate MOSFET.

Then, coating process takes place using a positive photo resist layer. After that ultraviolet (UV) light illumination is done followed by chemical removal of solvable regions as a result of UV radiance - lithography. Subsequently, one more chemical solvent is applied towards the surface of wafer to etch the regions which are required by photoresist followed by etching the remaining photoresist. This is shown in Figure 3 (e).

Next, coating of previous configuration with polysilicon is done in order to develop a gate electrode, transiting via planarization phase and then it terminates with what is shown in Figure 3 (f).

Afterwards, a layer of photoresist is applied. Followed by it, masking via lithography is done on top of it and then removal of solvent by a chemical reactant is done which reacts only with vulnerable region of gate electrode. Here we obtain a tri-gate MOSFET (SOI).

Fabrication of Tri-Gate Transistor

After that, we do more etching to remove the regions that are not covered by the unsolved photoresist after UV illumination and then residual photoresist covering the gate region is etched out. The finished structure is shown in Figure 3 (g) to (h).

Lastly, process of doping occurs to profile the fins of source and drain as illustrated in figure 3 (i).

Interview with the Company

The interview took place as follows:

What kind of Tri gate transistors are manufactured in your industry and what are their applications in appliances?

Answer: FinFET and UTB (Ultra-Thin Body) FET are the most common multi-gate transistors manufactured by semiconductor foundry. They offer enhanced gate control due to inherent better electrostatic compared to conventional planar FETs. FinFETs are 3-D devices with gate wrapped on three sides of the channel, which provides higher drive currents in the same footprint. This is the reason FinFETs are mostly utilized in high-performance chips like GPU (Graphical-Processing-Unit) for smartphones and high-frequency data serializers chip used in data centers. On the other hand, UTBFETs provide flexibility to tune threshold voltage using back gate bias, enabling transistor to operate in low leakage mode, which is essential for low-power IoT (Internet-of-Things) applications.

Moreover, UTBFETs are promising candidates for integrated RF & SoC applications because of its lower parasitics (like fringe capacitance and gate resistance) and non-volatile memory integration.

How reliable and efficient are these Tri gate transistors? What kind of problems are you facing with these transistors? How do you mitigate these problems?

Answer: FinFETs and UTBFETs show very efficient and reliable operation in their respective field of applications. However, for SoC (System on Chip) applications, the transistor needs to be a Logical Analog, RF, Memories (Volatil and non-volatile) components on the same chip. FinFET suffers from high parasitic capacitance and gate resistance, which makes it less attractive for RF applications. On the other hand, UTBFETs suffer from parasitic leakages (like GIDL, Gate Leakage, Impact Ionization) and high variability due to very thin silicon channel and mechanical stress. Moreover, reducing cost is challenging for both technologies. FinFETs require higher mask counts whereas UTBFETs need expensive SOI wafer.

The industry is still exploring ways to mitigate these issues. Further scaling of these transistors poses more challenges in reducing parasitics and controlling variability.

Interview with the Company

Are the current transistors being replaced by an tri-gate transistor which is more reliable and efficient than the present ones you are using?

Answer: Tri-gate transistors have successfully replaced conventional planar transistors for high-performance mobile applications and low-power IoT applications. GAA (Gate-All-Around) nanowire, pillar FETs are Tri-gate transistors which are being considered as future replacements.

What would be the future of tri-gate transistors in terms of application?

Answer: Tri-gate transistor will continue to improve its performance and cost with the introduction of new technologies (like Extreme-ultra-variability (EUV) lithography) and circuit techniques (like dynamic performance tuning).

Also, increase the level of integration will help these transistors to proliferate into the wider range of applications like automotive sensors, augmented reality, virtual reality and IoTs.

References


